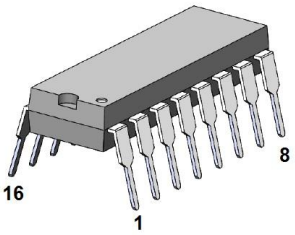
AS3310 - ADSR Voltage Controlled Envelope Generator

FEATURES

- Large Time Control Range: 100,000:1
- Full ADSR Response
- True RC Envelope Shape
- Exceptionally Low Control Voltage Feedthrough: 90µVmax
- Accurate Exponential Time Control Scales
- Isolated Control Inputs
- Good Repeatability and Tracking Between Units Without External Trim
- Independent Gate and Trigger
- Wide power supply range:
  negative rail: -15V ÷ -9V (via external resistor)
  positive rail: +11V ÷ +15V

APPLICATIONS
for electronic music

AS3310
PDIP-16 (300 Mil)



AS3310D
SOIC-16 (150 Mil)

General Description

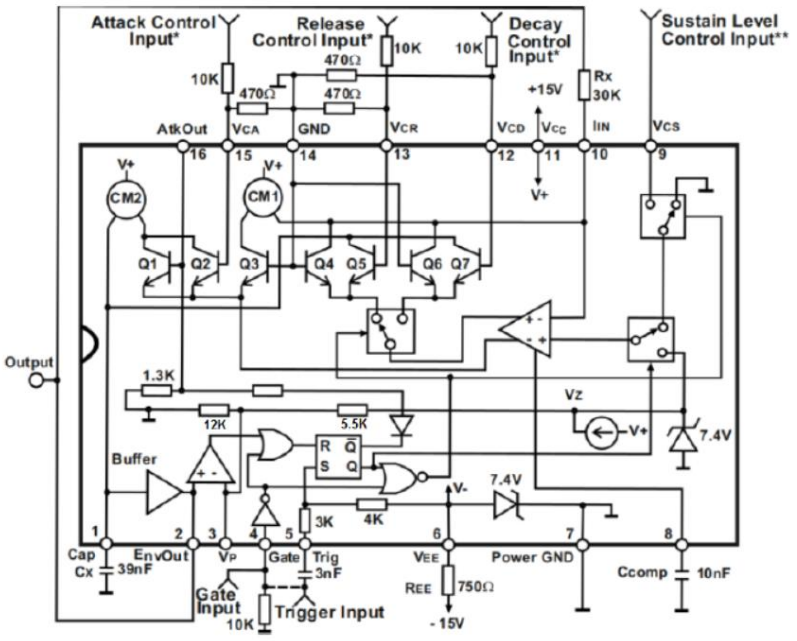
The AS3310 is a self-contained, precision ADSR type of envelope generator intended for electronic music and other sound generation applications. Attack, decay and release times are exponentially voltage controllable over a wide range, and the sustain level is linearly voltage controllable from 0 to 100% of the peak voltage Vp. All four control Inputs are Isolated from the rest of the circuitry so that the control pins of tracking units may be simply tied together.

On the negative power output, there is an internal Zener diode at 7.4 volts ± 10%, which allows the chip to supply a maximum voltage of ± 15 volts with a current-limiting resistor R_{EE}, and a minimum positive supply voltage of + 11 volts and a minimum negative supply voltage of -5 volts.. A series current limiting resistor must be added between pin 6 and the supply. Its value is calculated as follows: $R_{EE} = (V_{EE} - 7.5) / 0{,}010$

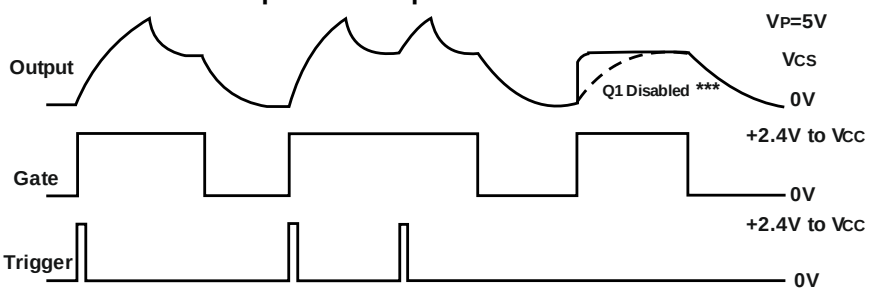
Pin Information

PDIP-16, SOIC-16 Pin No	Pin Name	Description
1	Cap	Capacitor
2	Env Out	Output
3	V_P	Attack Peak Input
4	Gate	Gate Input
5	Trig	Trigger Input
6	V_{EE}	Negative supply
7	Power GND	Power Ground
8	Ccomp	Compensation
9	V_{CS}	Sustain Level Control Input
10	I_{IN}	Input Current
11	V_{CC}	Positive supply
12	V_{CD}	Decay Control Input
13	V_{CR}	Release Control Input
14	GND	Ground
15	V_{CA}	Attack Control Input
16	Atk Out	Attack Output

Circuit Block and Connection Diagram



Input and Output Waveforms



*** Zero to -5V Varies the Times from 2mS to 20S**

****Zero to +5V Varies the Sustain Level from 0 to 100%**

*****Q1 Disabled if only a gate is applied with no trigger**

Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	24V
Voltage Between V_{CC} and GND Pins	+18V
Voltage Between V_{EE} and GND Pins	-6.5V
Current Into V_{EE} Pin	±50mA
Voltage Between Control and GND Pins	±6V
Voltage to Gate and Trigger Input Pins	V_{EE} to V_{CC}
Operating Temperature Range	- 25°C to 75°C

Typical Electrical Characteristics V_{CC}=+15V V_{EE} = -6,5 to -15V R_X= 30K T_A= 25°C

Parameter	Min.	Typ.	Max.	Units
Time Control Range	50 000:1	100 000:1	-	
Attack Asymptote Voltage (V_Z)	6.5	7.0	7.5	V
Attack Peak Voltage (V_P)	4.7	5	5.5	V
Attack Peak to Asymptote Tracking	-	1.5	4	%
Control Scale Sensitivity	58,5	60	61,5	mV/decade
Tempco of Control Scale	+3000	+3300	+3600	ppm
ATK, DCY, RLS Scale Tracking	-300	0	+300	µV/decade
Exponential Full Scale Control Accuracy[1]				
50nA < I_O <50µA	-	0.3	1.5	%
2nA < I_O < 200µA	-	2	10	%
Attack C.V. Feedthrough[2]	-	6	90	µV
Decay C.V. Feedlhrough[2]		NONE		
Release C.V. Feedtnrough[2]		NONE		
Sustain Final Voltage Error (V_O-V_{CS})	-3	+10	+23	mV
Release Final Voltage Error (V_O)	-3	+10	+23	mV
RC Curve Asymptote Error[3]				
V_{CA}, V_{CD}, V_{CR} = 0	-	-6	-60	µV
V_{CA}, V_{CD}, V_{CR} = -240mV	-	-125	-1250	mV
Input Current (I_{IN}) to Output Current (I_O) Ratio, V_{CA}, V_{CD}, V_{CR} = 0 [5]				
Charge Current (ATK)	0.75	1	1.3	
Discharge Current (DCY, RLS)	0.83	1	1.2	
Buffer Input Current (I_{B2})	-	0.5	5	nA
Op Amp Input Current (I_{B1})	150	400	800	nA
Gate Threshold	2	2.3	2.6	V
Gate Input Current	5	25	100	µA
Trigger Pullse Required to Trigger Envelope	+1.1	+1.3	+1.5	V
Trigger Input Impedance	2.4	3	4	KΩ
Time Control Input Current	0.5	-	2500	nA
Sustain Control Input Current	150	400	800	nA
Attack Output Signal	-0.4	-0.8	-1.2	V
Output Current Sink Capability	0,42	0,56	0,7	mA
Buffer Output Impedance	100	200	350	Ω
Positive Supply Range	+11	-	+18	V
Negative Supply Range [4]	-4.5	-	-18	V
Supply Current	5.6	7.5	9.4	mA

Note 1**:** Scale factor determined at mid-range. Spec represents total deviation from ideal at range extremities.
Note 2**:** Output is at either sustain final voltage or release final voltage. V_{CA}**,** V_{CD}**,** V_{CR} varies 0 to -240mV.
Note 3**:** Spec represents the difference between the actual final voltages (attack asymptote voltage, sustain final voltage, and release final voltage in the case of attack, decay, and release respectively) and the apparent voltage to which the output seems to be approaching asymptotically.
Note 4**:** Current limiting resistor required when V_{EE} > -7 volts.
Note 5**:** Spec also represents time constant variation between units for V_{CA}, V_{CD}, V_{CR} = 0**.**

Specifications subject to change without notice.

Application information :

Below are the equations for calculating the attack, decay and release phase envelopes.

Envelope equations:

Attack Curve

$$V_{OA} = V_Z \left(1-\exp\left(-\frac{t}{RxCx} e^{V_{CA} / V_T}\right)\right)$$

Decay Curve

$$V_{OD} = (V_P - V_{CS}) \exp\left(-\frac{t}{RxCx} e^{V_{CD} / V_T}\right) + V_{CS}$$

Release Curve

$$V_{OR} = V_{CS} \exp\left(-\frac{t}{RxCx} e^{V_{CR} / V_T}\right)$$

Sustain /Release Final Voltage Error

$$E_F = V_{OS} + I_{B1}R_X - I_{B2}R_X / 1 + e^{V_{CA} / V_T}$$

Attack/Decay/Release Asymptote Error

$$E_A = V_{os} + I_{B1}R_X - I_{B2}R_X\, e^{-V_{CA,D,R} / V_T}$$

V_{CA} = Attack Control Voltage
V_{CD} = Decay Control Voltage
V_{CR} = Release Control Voltage
V_{CS} = Sustain Control Voltage
V_{os} = Op Amp Offset
I_{B1} = Op Amp Input Current
I_{B2} = Buffer Input Current
V_Z = Attack Asymptote Voltage
V_P = Envelope Peak Voltage
$V_T = kT / q$

The peak currents of the charge and discharge of the capacitor Cx can be determined from the following expressions:

$I_{pA}=(V_Z / R_X) \exp(V_{CA}/V_T)$
$I_{pD}=(V_{CS}/R_X) \exp(V_{CD}/V_T)$
$I_{pR}=(V_P/R_X) \exp(V_{CR}/V_T)$

for the attack, decay and release phases, respectively.

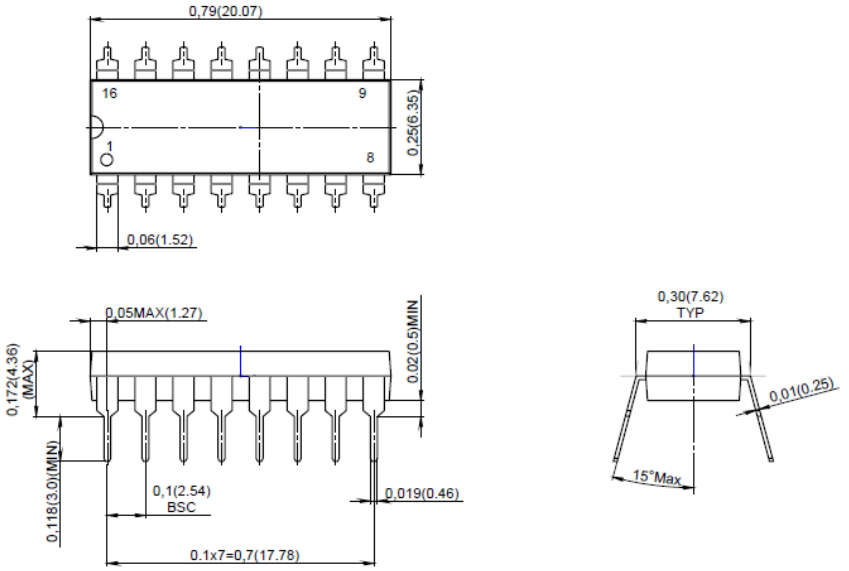
For example, the maximum peak attack charge current I_{pA} will be at $V_{CA}=0$. You can calculate the maximum peak attack current I_{pAmax} by substituting in the equation $I_{pA}= (V_Z/R_X)\exp(V_{CA}/V_T)$ the corresponding values $V_{CA}=0$, $V_Z=7.4V$, $Rx=30K$, $I_{pAmax}=Vz/Rx=7.4V/30K=247\mu A$

Package Information

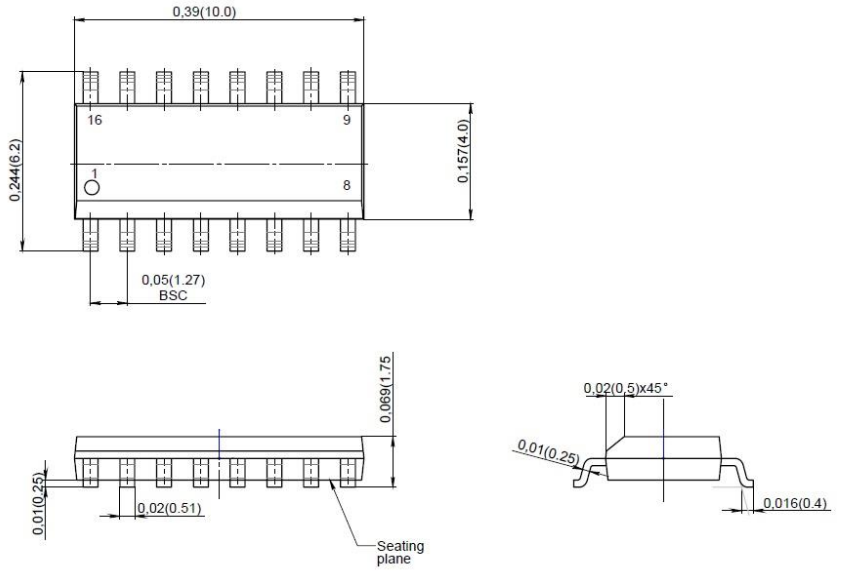
Device type	Package
AS3310	PDIP-16 (300 Mil body)
AS3310 D	SOIC-16 (150 Mil)

Units: inch (mm)

PDIP-16 (300 Mil)



SOIC-16 (150Mil)



Revision history

Date	Revision	Changes
27-Sep-2017	**1**	Preliminary version 1
21-Oct-2017	**2**	Minor changes: Ccomp=10nF
29-Nov-2017	**3**	Changes in supply and attack levels
19-Dec-2017	**4**	Changes in Description and Block Diagram
21-May-2018	**5**	Minor changes
30-Sep-2019	**6**	Minor changes: Rx=30K
22-Feb-2023	**7**	Application information added