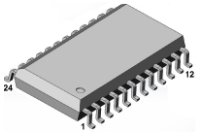
AS3052 NPN Transistor Array

Features

- 8 matched npn transistors, 2 diodes, 1 burried zener diode
- V_{BE} matched less than ±1 mV
- wide operating current range

AS3052 D



SOIC-24, 300mil, 1.27 pitch

Applications

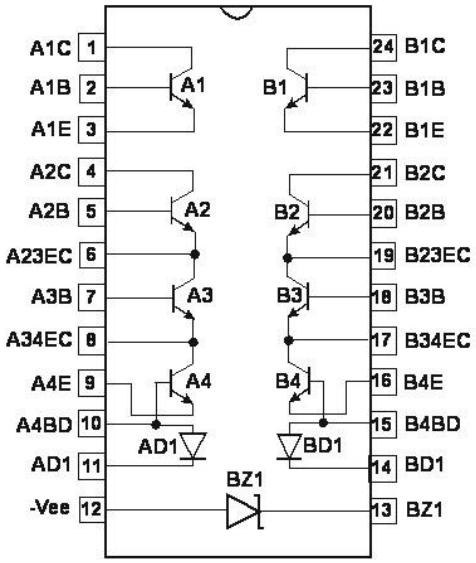
- filters (Moog type)
- multipliers (like MC1496)
- dividers
- Gilbert cells
- custom designed differential amplifiers
- temperature compensated amplifiers

General Description

The AS3052 consists of 8 NPN transistors, 2 diodes and 1 buried zener on a common monolithic substrate. Transistor array allows variety of connections – differential pairs, different type of current sources, and different kind of multipliers/dividers. They may be used as discrete transistors in conventional circuits, however in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Pin 12 (-Vee, substrate) must be connected to lowest potential in circuitry. Diodes AD1 and BD1 are formed from transistors similar to A1-A4 (B1-B4).

Connection Diagram
Top View



AS3052 D

Pin Information

Pin number	Description	Pin number	Description
1	Collector A1C	24	Collector B1C
2	Base A1B	23	Base B1B
3	Emitter A1E	22	Emitter B1E
4	Collector A2C	21	Collector B2C
5	Base A2B	20	Base B2B
6	Emitter A2/ Collector A3	19	Emitter B2/ Collector B3)
7	Base A3	18	Base B3
8	Emitter A3/ Collector A4	17	Emitter B3/ Collector B4
9	Emitter A4	16	Emitter B4
10	Base A4/ Anode AD1	15	Base B4/ Anode BD1
11	Cathode AD1	14	Cathode BD1
12	-Vee (substrate)	13	Cathode Zener BZ1

Absolute Maximum Ratings	Each Transistor	Total Package	Units
Power Dissipation	200	500	mW
Collector-Emitter Voltage, U_{CEO}	30		V
Collector-Base Voltage, U_{CBO}	50		V
Collector-Substrate Voltage, U_{CIO} (Note 1)	50		V
Emitter-Base Voltage, U_{EBO}	5		V
Collector-Current, I_C	30		mA

NOTES:

1. The collector of each transistor of the AS3052 is isolated from the substrate by an integral diode. The substrate (Pin 12) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

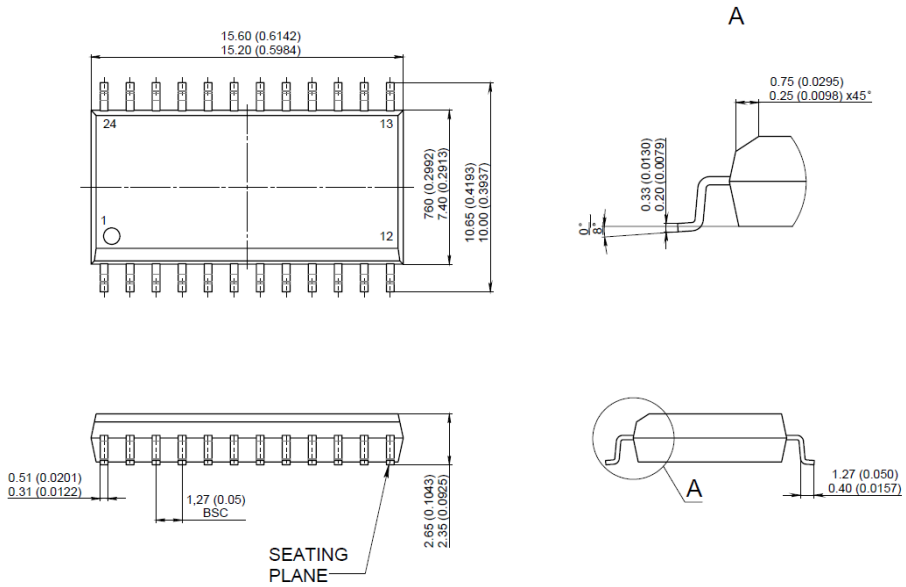
Electrical performance characteristics (Tj = +25C)

Parameter	Conditions	Min	Typ	Max	Units
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10μA, I_E = 0	50			V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 100μA, I_B = 0	30			V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10μA, I_{CI} = 0	50			V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E = 10μA, I_C = 0	5	6,5		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0,002	5	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			20	nA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE}=3V, I_C=10mA	150			
	V_{CE}=0V, I_C=1 mA	150			
	V_{CE}=3V, I_C=10μA	140			
Input Offset Current for Matched Pair A1/A2 (B1/ B2) $\lvert I_1 - I_{I2}\rvert$	V_{CE} = 3V, I_C = 1mA		0,02	1	μA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1mA			0,75	V
	I_E = 10mA			0,8	
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$ A1/A2 , B1/B2	V_{CE} = 3V, I_C = 1mA		0,5	1	mV
Magnitude of Input Offset Voltage for Transistors $\lvert V_{BE1} - V_{BE2}\rvert$, $\lvert V_{BE2} - V_{BE3}\rvert$, $\lvert V_{BE3} - V_{BE4}\rvert$	V_{CE} = 3V, I_C = 1mA		0,5	1,5	mV
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B =1 mA, I_C =10mA		0,1	0,15	V
Zener voltage breakdown (1 mA)			7,2		V

Device type	Package
AS3052 D	SOIC-24, 300mil, 1.27 pitch

Package Information

24-Lead Standard Small Outline Package (SOIC_W)
Wide Body
Dimensions shown in millimeters and (inches)



Revision history

Date	Revision	Changes
12-Dec-2019	**1**	Preliminary version 1
11-Jan-2021	**2**	Package information updated